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PERFORMANCE OF LEAKAGE POWER MINIMIZATION TECHNIQUE FOR CMOS VLSI TECHNOLOGY

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ABSTRACT

Because of the quick advancement of semiconductors equipment and the rising require for battery-powered moveable gadgets, designers have scaled down feature sizes, resulting in lower The integration of exceedingly complicated functionalities on a single chip, as well as the threshold voltage. Chip's maximum power method is used in both technological and execution aspects. To expand the number of devices in a concert, three critical characteristics are required: system speed, small footprint, and low power usage. The total power utilization of integrated devices is resolute by leakage current dissipation in particular. The CMOS VLSI Technology's leakage power is a major issue. A Leakage Power Minimization the Technique is used in the research to decrease outflow Power in CMOS devices. Currents of leakage are tracked and compared. The Charge is initiated by the Comparator. Pumping blood to the body (V body). These circuits have been modeled. This was accomplished with the help of TSMC 0.35m technology and diverse operational conditions. The current steered digital-to-analog converter is known as CSDAC (Steering Digital-to-Analog Converter). As a proof of concept, it's being used as a test core. Core of the test (eg.8-bit CSDAC).It consumed 347.63 mill watts of power. The LPMT circuit alone uses a significant amount of energy.6.3405 mW in power Leakage is reduced when this technique is used.

Keywords: CMOS, Leakage power, current steering, test core.

INTRODUCTION

The evolution of digital integrated circuit that is held up by high Power Consumption. A grouping of greater timer speed more combination and functionality minor manufacturing graphs have resulted in a major boost in power density. On a chip, scaling increases transistor density and functionality. Scaling allows you to enhance the frequency and speed of your activities, resulting in better result. Threshold voltages have to also fall to gain the performance benefits of new technology, voltages must scale downward with geometries, while leakage current increases exponentially. As oxides of the gate thinned, gate leakage current has grown. In recent years, Leakage power in the CPU hardware & software design has become a major problem. With a decreased instrument size, the primary element of the leak is the low threshold current, with increasing energy consumption. The CPU the power consumption is increased exponentially. Leakage accounts for about 30-40% of the CPU power with 65 nm and below technology. As the size of the technological characteristics decreases such as the International Technology Roadmap for semi-conductors. The dissipation of leaking power may occur at some point. eclipse total power expenditure. While there are a variety of circuit-level technology and process technologies ways for minimizing outflow

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in processors, this research provides the number of narrative ideas using the lowest feasible space and delay trade-off for minimizing leakage and dynamic power Leakage Power excess has become a significant issue used for VLSI circuit designers with the latest CMOS element size . CMOS power Consumption is influenced by both dynamic & static components. When transistors switch, Regardless of transistor flipping, dynamic and static power are used.

Dynamic Power is responsible for 90% or more of overall chip power (at 0.18 technology and even beyond), making it the single most critical concern for lowpower chip designers in the past. As a result, many previous proposals, The goal of voltage and frequency scaling were to reduce Dynamic Power. As characteristic sizes shrink to 0.09 and 0.065, static power has happen to a serious concern in terms of present and future technologies.

Technology scaling has been one of the impetuses for the considerable gains in performance, functionality, and power in integrated circuits over the previous few years.

Power loss have become an important parameter as a result of downsizing and the Wireless communication is becoming more popular. Deep-submicron technologies reduce Transistors' supply voltages and threshold voltages have been substantially .The minimizes the dissipation of dynamic (switching) power to some extent. The sub threshold leakage current are boosts Static Power dissipation exponentially. The current that passes through a transistor when it is turned off is referred to as leakage current. It is influenced by gate length & oxide thickness, and that changes exponentially as a function of threshold voltage, temperature, and other factors.

Modern digital circuitry is made up of logic gates CMOS technology are used. The two kinds of power consumption are Dynamic Power and leaky power [2]. When the circuit performs a function and the signals vary, dynamic power is used. Even when a circuit is turned off then static power also known as leakage, is consumed continuously. It's unnecessary, and it'd be better to get rid of it [3]. Sub-threshold flow rates will account for a greater proportion of overall power dissipation as scaling and power reduction tendencies in future technologies continue.

The key determinant of leakage power is sub-threshold leakage current, that rises as a threshold voltage falls. Several approaches have been proposed to limit leakage power, gadget size, multi-V^{th} & dual-V^{th}, best standby input vector choice, stacking circuits, dual Vdd, and so on.

High performance and increased packing densities characterise modern digital integrated circuits (ICs). This is owing to the strong device scaling. That occurs in If device physics remain constant, this will happen For a few more years, every technological generation. Higher integrating is more cost-effective since it lowers the cost of connection and packaging by reducing the number of elements per system. Furthermore, it improves the whole system's reliability. Because parasitic interactions in

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devices and interconnections are reduced, Higher integration speeds up a circuit. Today, one of the main design problems is power usage alongside space, performance, cost and yield, with the rapid rise is manageable, digital equipment that is powered by a battery such as well as cell phones, laptops, special digital assistants, multimedia devices and so on. The battery's life, on the other hand is limited. Despite notable advancements advancements in High-capacity rechargeable Lithium-ion cells for example, battery technology. the prospect of it's unlikely that battery technology will undergo a significant change in the foreseeable future. In these conditions, the only the usage of a power-saving device is one method to decrease power consumption certain cutting-edge low-power circuit design techniques. Furthermore, while the circuit or its constituent pieces are inactive, unnecessary power dissipation must be limited via dynamic power management techniques. There are numerous benefits to optimising a circuit's power consumption. Because the core is less heated, it aids in the development and usage of less expensive packaging and cooling. This is crucial from the standpoint of the system's overall cost, and as a result, low-power strategies are now being used on desktop and workspace computers to minimize cooling and packing costs.

From the system and architectural level to the physical level, more attention is placed on each step of the design cycle. to achieve low power usage. On the other side, the cost of production is dictated not only by volume, as well as by design styles, projected application, circuit design, and time-to-market and manufacturing quality. In actuality, only a few circuit such as some general-purpose CPUs, having a large sales volume and a lengthy lifespan, but technological advances swiftly render them obsolete. Application Specific Integrated Circuits are intended to execute a specific set of activities and account for a significant percentage of the market.

Optimisation of circuits for particular quality and a decrease in design time necessitates the use of computer-aided design (CAD) methods. As the level of integration continues to develop, the task of completing a thorough design without flaws becomes Human designers are finding it more challenging. As technology advances, More cores & processors are being added. crammed into smaller SoC devices (Kaur, 2013). The vast majority of these high-performance systems require a lot of power. Since the origin of integrated circuits, CAD tools have been utilized. With its expanding capabilities, CAD techniques have progressed in many domains and will continue to facilitate the design of increasingly larger circuits. Because dynamic or switching power is related to the square of the voltage provided, the supply voltage is constantly scaled down to minimise power usage.

To prevent any performance degradation, scaling the power supply will also need the threshold voltage. In long channel devices, leakage power is unimportant. Because the sub-threshold leakage is expanding related to threshold voltage, decreased threshold voltage leads to a growing consumption of leaking power. In addition to 100 nm devices, the Leakage Sub-threshold exceeds all other leakage. In technology under 90 nm oxide leakage & tunneling tape to band leakage predomine. Recent technological

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developments have made the leakage power consumption equivalent to dynamic energy consumption. In many applications, the Power Consumption is much greater than Dynamic Power Consumption. This would emphasize leakage Power Consumption over and above a Dynamic Power Consumption untimely on in the design cycle. Figure 1 shows that increasing trend of power dissipation in line with the ITRS (http://www.itrs.net). Figure 2 shows the increase in power dissipation.

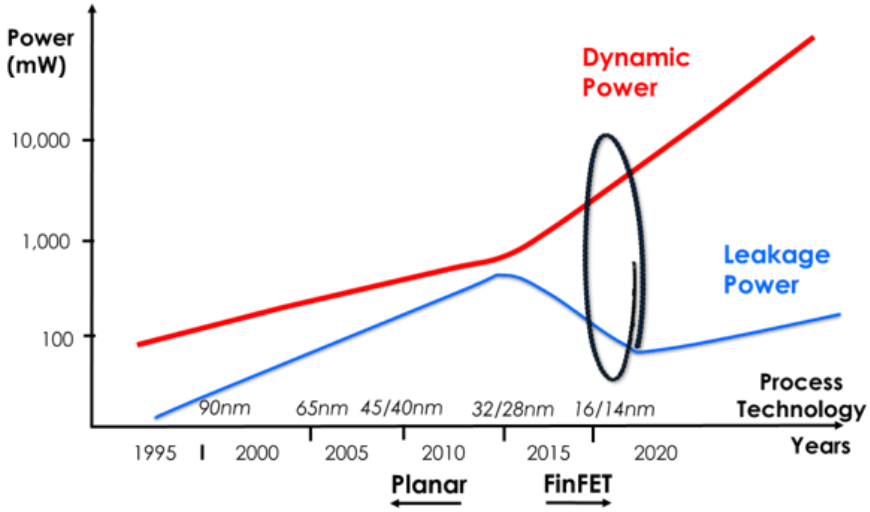

Fig. 1. ITRS SoC-CP Power Consumption Trends.

RELATED WORK

Most suggested an alternative leakage power reduction technique. These are discussed in the following order: Few have concentrated on the sleep transistor technique [10]–[13]. By shutting off the power sleep transistors are disabled during the sleep form. By turning of the power source in the circuit design, the leakage power in the power source was minimized. In sleep mode, however, this results in state annihilation as well as a floating output voltage. Additionally, by extending the time it takes to wake up to the maximum, this strategy lowers delay by using the sleep mode sleep minimization. The sleepy stack approach is established in existing literatures [12], [14]. For the planned sleepy state architecture, In sleepy stats, the stack effect transistors are split into two separate transistors of half-length. These classify Transistors are linked in a parallel design to the transistor that acts as a dividend. Leakage current is suppressed by the stacking transistor in sleep mode/saving mode by revolving off the sleep transistor. Since every transistor is replaced with three transistors, the product penalty of power delay plays a large part in this strategy. For minimizing sub-threshold leakage current reduction, a sleepy stack strategy is constructed by combining transistor stacking with a sleep approach [15], [16]. The transistors are divided into two halves during stacking, This increase the circuit's resistance and connects sleep transistors in parallel, which

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reduce the ISUB exponentially. The major advantage of The logic of the circuits without rail is preserved in this circuit. by V_{DD} and the primary drawback is that high V^{th} T cannot be used. When the fast speed approach employs either On & Off method in the sleep form with two sleep pull-ups or pull-downs independently. By using this double sleep section for the entire circuit design, certain logical circuits require a small number of transistors [19]. Compared to earlier tests, more power delays are needed, which may degrade the delay of the circuit.

3. LEAKAGE POWER MINIMIZATION TECHNIQUE

There are four stages to the leakage power minimization technique:

1) Leakage current monitor,

2) Current compare,

3) Charge force,

4) Test core (CSDAC).

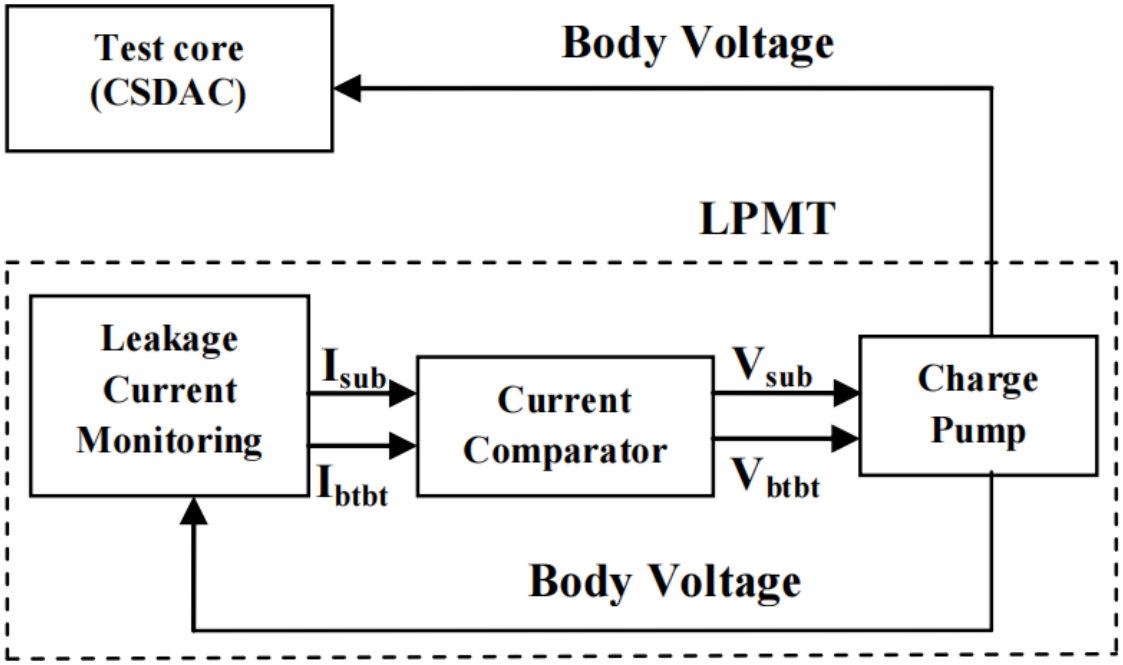

Fig.2. LPMT system

Leakage currents are depicted in Figure 2. In stage 1, Isub and Ibtbt are monitored. In the next stage the current comparator outputs the compared leakage current values. Stage 3 generates Core strength is measured using body voltage (CSDAC).

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3.1 LEAKAGE CURRENT MONITORING

All elements of the current leakage mechanism in CMOS VLSI technologies are current threshold band to band tunneling and the gateway toward bulk oxide tunneling current. CMOS transistor with all the leakage current parts are shown in Fig.3.

In CMOS devices, power leakage is mostly caused by the sub-threshold & band to band current.

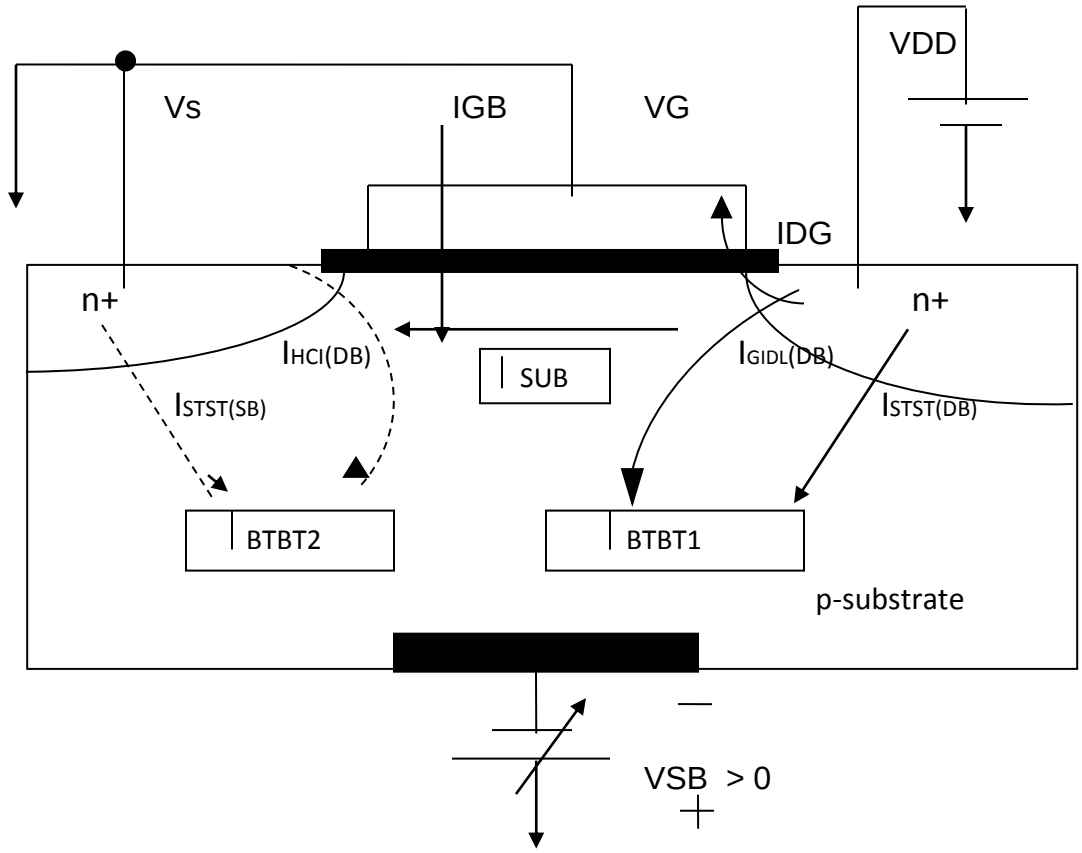

Fig.3. Leakage Current Components in MOS

The ISUB and BTBT leakage (ITBT) components are segregated by the leakage surveillance circuit from the overall leakage components. Sub threshold leakage that is minimized when two or more stacking transistors are used. The amount of off transistours in the stack is determined by the input pattern during idle intervals this minimization is a function of it.

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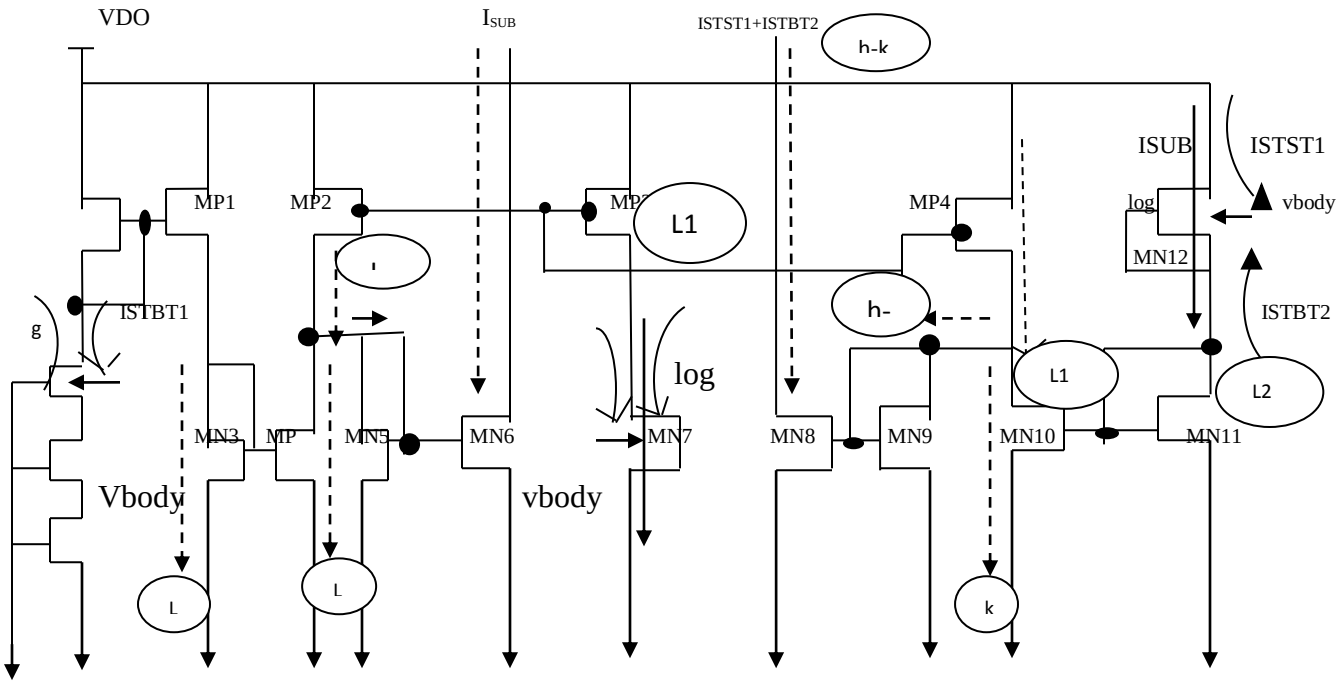

Fig.4. Leakage Current Monitoring Circuit

The ISUB & BTBT leakage stream (IBTBT 1 and 2) are separated by the leak monitoring systems from the total leak parts. Figure 4 shows the new MN2, MN7, and MN12 CMOS Leakage Monitor (CMOS) circuits, while the actual MP0/MP1, MP2/MP3, MN10/MN11 mirrors are the transistors.

To avoiding three transistors, we may disregard the sub-threshold current is fluid from the transistor's consume to its resource. As a result, MN2 transistor drainage current known as I2, is nearly as same IDG and IBTBT1. The MN7 drain current, designated as 11, consists of IDG, IBTBT1 and ISUB. In the MN12 transistor source, current 13 is generated by IDG, IBTBT2, and ISUB. The leakage monitoring circuit for the PMOS device is similar to the NMOS device's monitoring circuit.

Based on the leakage components that occur, two current differential speaker are used. MN4, MN5, and MN6 transistors generate ISUB (current I1–current I2), while MN8, MN9, and MN10 transistors produce IBTBT=IBTBT1+IBTBT2 (current I1–current I3).

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The current comparators are utilized for the application of the individual leak components for the pulse width of each leakage. The charging pump then unloads or charge its output condenser based on the two signals and the bias voltage from the current comparator. The current design based on the comparator provides ISUB and IBTBT with the best possible body-bias voltage[1].

4. DESIGN PROCEDURE

The design of low-power circuits have become a hot topic in the electronics industry these days. As a result, the necessity for this low power has resulted in a considerable shift in perspective, whereby power dissipation is a crucial element in area and performance discussion. This section presents novel techniques to reducing leakage power, as well as simulations to go along with them. The following are the points that will be discussed:

A. Proposed method

This research proposes a unique method to reduce power leak in VLSI circuits using CMOS circuits. In conjunction with the LECTOR transmitter the new method is sleepy. A circuit diagram appears into Figure 5. The proposed technology use the aspect ratio of W/L=2 for a PMOS circuit transistor. On the other hand, the aspect ratio of a transistor is W/L = 1. Sub-threshold value is minimized by using the circuit's minimal aspect ratio. The sleep transistors are employed in this technique to differentiate the ground and power source. Apart from it, the gate is connected to the remaining transistors. It is controlled by the input vector and In both active and inactive phases, switches slumber transistors, costing power. A logic circuit based on a pull-up and pull-down network circuit also uses the two transistors. Transistors are connected to deal with input combinations by placing any one of them near the cut-off voltage. The route resistance for the ground to supply link will be provided by this transistor arrangement. This resistance ensures that the circuit's leakage current is kept to a minimum. The developed circuit will work successfully Both active and standby modes are supported. Increase the resistance all the way to the ground from the source.

The VCC and GND terminals of transistors are used to design the system array. Self-controlled voltage technique is the name given to such a system. It is built in such a way that, It saves energy by enabling transistors to switch between safe voltage levels in order to avoid overheating. The Power dissipation across the transistors is significantly lowered when the leakage current is minimised.

Layout Design

The integration of NMOS by n+ gate & diffusion layer by insertion of Poly-Silicon is given in the layout design of transistors. The designed circuit was also connected to metal-1 and metal-2 for completion. In this constructed circuit, read and write operations can be conducted on the active word line. When a word line is not active, the intended circuits operate as an open circuit is not active.

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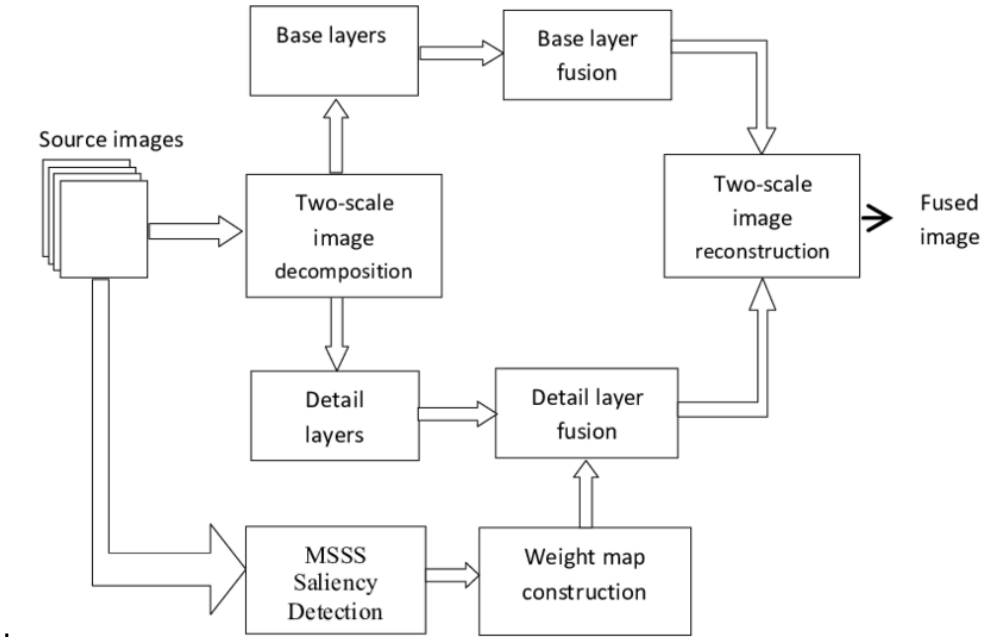

Fig.6. Block Diagram of proposed method

Figure 6 depicts a potential architecture design that includes the LECTOR stack for power usage. For power consumption reduction, this proposed technique employs a logic design that combines pull - up & pull - down logic. The sleepy signal is fed into Vcc via a parallel connection with a pull - Up & pull - down logic circuit, which feeds the waveform of the sleepy signal to both transistors. The proposed method is put into practice in VLSI circuit design, and the results are evaluated.

5. SIMULATIONS AND RESULTS

This segment includes simulation of the suggested methods. To generate simulations, the Microwind Tool is utilized. Compiling the Verilog file in Microwind 3.1 is the first step towards obtaining the simulations. The circuit diagram that was produced in the schematic is converted into a Verilog file. Microwind 3.1 now compiles the Verilog file. Microwind will produce the layout for the circuit diagram generated in diagram once the Verilog file has been prepared. The arrangement is then subjected to simulations.

Figures 7 demonstrate simulation of the projected methods. The waveforms of Voltage, Time and Voltage Current are presented in these simulations. Figure 7 shows the comparable simulations of the sleep transistor technique using NMOS. The performance gained from the sleep transistor approach using NMOS is good when compared to the standard sleep transistor advance, as can be seen from the waveform. In this new approach, the delay is likewise reduced, and the maximum current is increased.

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Figure 8 shows simulations of a sleep-forced NMOS stack. In comparison to strategies such as stack, sleepy keeper, and sleep transistor approach, this novel strategy features a maximum current, low power consumption, and excellent performance.

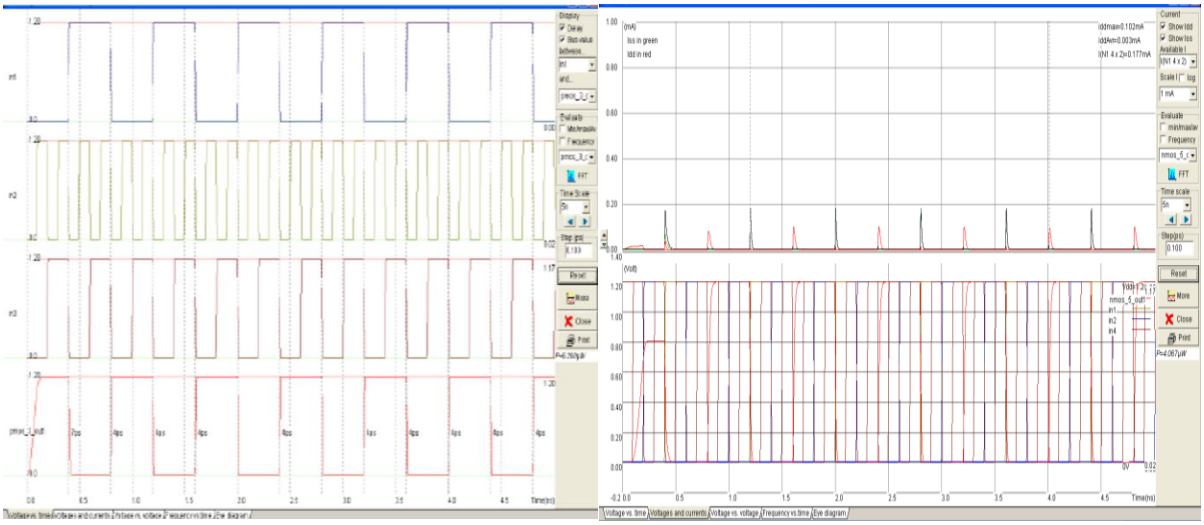

Fig 7: Sleep Forced NMOS Stack

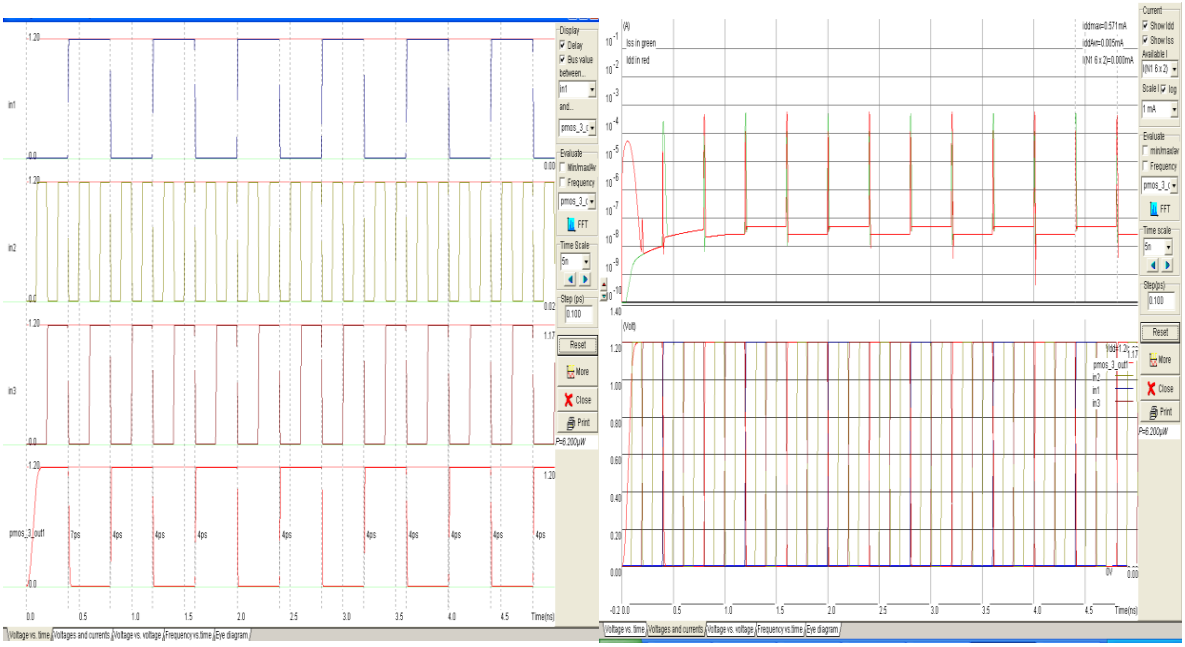

Fig8: Variable Body Biasing with Bypass

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The simulations of a variable body biassing with bypass approach are shown in Figure 8. In comparison to the base case and traditional procedures, this strategy has a shorter delay and a higher maximum. As illustrated in the waveforms, variable body, biasing with bypass has decreased the outflow current to a minimum.

6. CONCLUSIONS & ACKNOWLEDGEMENTS

The components of leakage current are monitored using a leakage monitoring circuit. Body voltage is generated using a charge pump, which serves as a feedback loop for testing the core and leakage current monitoring circuits in order to reduce power consumption. The LPMT system produces significant power savings across a wide temperature range. This pattern could also be applied to a wide range of process parameters. As a result, with finer technologies, this technique proven to be reliable in lowering leakage power.

Leakage current has increased as technology has been scaled down. In comparison to dynamic power, leaky power has become more prevalent in recent years. In low-power, high-performance digital CMOS devices, leakage current is a major issue. Effective techniques for minimising leakage current in VLSI design are given in this article. While preserving state, the suggested methods consume relatively minimal static power.

The proposed designs have a short latency and good performance. They are also more area efficient and have a smaller leakage current than conventional approaches. The technique that has been proposed is Variable body biassing with bypass is both power efficient and provides more maximum current than the basic case, which is an inverter, while also having Of all the methods investigated in this study, this one had the least leakage current. At ambient temperature, the findings were pretend by the Microwind 3.1 tool in 90nm technology.

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